

Amendments to the Claims

1. (Original) A search algorithm for a successive-approximation-register (SAR) analog-to-digital converter (ADC), comprising:

initializing each of N three-way elements of a digital-to-analog converter (DAC) for a SAR ADC to a middle reference voltage wherein the N three-way elements of the DAC are each able to be set to one of three values; and

determining and setting the each of the N three-way elements from the middle reference voltage to either a high reference voltage or a low reference voltage depending upon a comparison result between an analog input value of the SAR ADC and a DAC voltage value of the DAC.

2. (Original) The search algorithm according to Claim 1, wherein the determining and setting step further comprises:

determining whether the analog input value is greater than the DAC voltage value based on element values of the DAC;

in response to the analog input value being greater than the DAC voltage value, switching a three-way element to be switched from the middle reference voltage to a high reference voltage; and

in response to the analog input value not being greater than the DAC voltage value, switching the three-way element to be switched from the middle reference voltage to a low reference voltage.

3. (Original) The search algorithm according to Claim 2, further comprising:

setting an element count value to an N value wherein the three-way element to be switched from the middle reference voltage is the element corresponding to the element count value;

performing the determining and switching steps for the element corresponding to the element count value in setting the three-way element from the middle reference voltage to either the high reference voltage or the low reference voltage; and

subtracting the element count value by one and repeating the determining and switching and subtracting steps for setting each of the N three-way elements from the middle reference voltage to either the high reference voltage or the low reference voltage until the element count value equals zero.

4. (Original) The search algorithm according to Claim 3, wherein the initializing and switching steps further comprises:

three-way switching each of the N three-way elements to either the middle reference voltage, the high reference voltage, or the low reference voltage.

5. (Original) A successive-approximation-register (SAR) analog-to-digital converter (ADC), comprising:

a digital-to-analog converter (DAC) having N three-way elements wherein the DAC converts digital signals to analog signals and N is an integer greater than one;

a register coupled to the N three-way elements wherein each of the N three-way elements is able to be set to one of three values;

three-way switches that three-way switch and couple each of the N three-way elements to either a high reference voltage, a middle reference voltage, or a low reference voltage;

a successive-approximation-register (SAR) logic system coupled to the register;
and

a comparator for receiving and comparing an analog input value and a DAC output value from the DAC and for providing a comparator output signal that is fed into the SAR logic system.

6. (Original) The SAR ADC according to Claim 5, wherein the SAR logic system:

initializes each of the N three-way elements of the DAC to a middle reference voltage; and

determines and sets the each of the N three-way elements from the middle reference voltage to either a high reference voltage or a low reference voltage depending upon a comparison result between the analog input value and the DAC output value.

7. (Original) The SAR ADC according to Claim 6, wherein the SAR logic system further:

determines whether the analog input value is greater than the DAC output value based on elements values of the DAC;

in response to the analog input value being greater than the DAC output value, switches a three-way element to be switched from the middle reference voltage to a high reference voltage; and

in response to the analog input value not being greater than the DAC output value, switches the three-way element to be switched from the middle reference voltage to a low reference voltage.

8. (Original) The SAR ADC according to Claim 7, wherein the SAR logic system:

sets an element count value to an N value wherein the three-way element to be switched from the middle reference voltage is the element corresponding to the element count value;

performs the determination and switching for the element corresponding to the element count value in setting the element from the middle reference voltage to either the high reference voltage or the low reference voltage; and

subtracts the element count value by one and repeats the determination and switching and subtraction for setting each of the N three-way elements from the middle reference voltage to either the high reference voltage or the low reference voltage until the element count value equals zero.

9. (Original) The SAR ADC according to Claim 8, wherein the SAR logic system further:

three-way switches each of the N three-way elements between either the middle reference voltage, the high reference voltage, or the low reference voltage.

10. (Original) A successive-approximation-register (SAR) algorithm for a SAR logic system of a SAR analog-to-digital converter (ADC), comprising:

- a. a memory medium; and
- b. a successive-approximation-register (SAR) algorithm stored on said memory medium, said SAR algorithm comprising instructions for:
 - i. initializing each of N three-way elements of a digital-to-analog converter (DAC) for the SAR ADC to a middle reference voltage wherein the N three-way elements of the DAC are each able to be set to one of three values; and

ii. determining and setting the each of the N three-way elements from the middle reference voltage to either a high reference voltage or a low reference voltage depending upon a comparison result between an analog input value of the SAR ADC and a DAC voltage value of the DAC.

11. (Original) The SAR algorithm according to Claim 10, wherein the determining and setting instruction further comprises instructions for:

determining whether the analog input value is greater than the DAC voltage value based on element values of the DAC;

in response to the analog input value being greater than the DAC voltage value, switching a three-way element to be switched from the middle reference voltage to a high reference voltage; and

in response to the analog input value not being greater than the DAC voltage value, switching the three-way element to be switched from the middle reference voltage to a low reference voltage.

12. (Original) The SAR algorithm according to Claim 11, further comprising instructions for:

setting an element count value to an N value wherein the three-way element to be switched from the middle reference voltage is the element corresponding to the element count value;

performing the determining and switching instructions for the element corresponding to the element count value in setting the element from the middle reference voltage to either the high reference voltage or the low reference voltage; and

subtracting the element count value by one and repeating the determining and switching and subtracting instructions for setting each of the N three-way elements from the middle reference voltage to either the high reference voltage or the low reference voltage until the element count value equals zero.

13. (Original) The SAR algorithm according to Claim 12, wherein the initializing and switching instructions further comprises the instruction for:

three-way switching each of the N three-way elements between either the middle reference voltage, the high reference voltage, or the low reference voltage.

14. (Currently amended) A three-way element for a digital device, comprising:

an element having at least three states and wherein the at least three states include at least a low state, a middle state, and a high state; and

wherein the three-way element having the at least three states is utilized in conjunction with a three-way switch that three-way switches and sets the three-way element to one of the at least three states.

15. (Original) The three-way element for a digital device according to Claim 14, wherein the middle state is utilized as an initial state by a successive-approximation-register (SAR) algorithm and the SAR algorithm determines whether the three-way element is to be switched from the middle state to either the low state or the high state.

16. (Original) The three-way element for a digital device according to Claim 14, wherein the three-way element having the at least three states is utilized in a digital-to-analog converter.

17. (Original) The three-way element for a digital device according to Claim 14, wherein the three-way element having the at least three states is utilized in a register.

18. (Cancelled).